Application No.: 10/777,599

Docket No.: JCLA12098

AMENDMENT

Please amend the application as indicated hereafter.

In the Specification

Please amend paragraph [0035] as follows:

[0035] FIG. 1 is a circuit diagram schematically illustrating a voltage level shifter according to one preferred embodiment of the present invention. Referring to FIG. 1, an inverter includes, for example but not limited to, a PMOS transistor 101 and a NMOS transistor 111. The output stage is provided by an inverter 131. The inverter 131 can be, for example, a high voltage inverter. A first control signal (VA') inputted to the AND gate 141 comprises, for example, a low voltage signal, and a second control signal (VA) inputted to the transistor 101 is adjusted to comprise a high voltage signal having the same phase as the first control signal (VA') inputted to the AND gate. The PMOS transistor 101 and the NMOS transistor 111 need to be activated at different times in order to break the current paths. FIG. 5 is a waveform diagram schematically illustrating the simplified input and output voltages of the voltage level shifter of FIG. 1. Referring to FIG. 5, the transistor 101 should be turned off before the transistor 111 is turned on when an input VIN (e.g., a clock TTL voltage signal) changes from low to high level. Thus, a control signal VA is input to the voltage level shifter, –in which a timing of the control signal VA is prior to the input VIN by a time period Tdis. The control signal VA, for example, can be a high voltage control signal. The state of VOUT1B prior to the Tdis is at an analog high voltage high level VDDA, and the state of VOUT1B during the period Tdis is at high impedance state. Thus, a capacitor 121 stores the original high level and an output stage of the voltage level shifter maintains its outputs to VOUT1 with an analog high voltage low level GNDA. The transistor 111 is turned on when VIN is at high level, thus the VOUT1B is pulled down to the analog high voltage low level GNDA and then the output stage outputs to VOUT1 with an analog high voltage high level VDDA.

Please amend paragraph [0038] as follows:

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[0038] FIG. 2 is a circuit diagram schematically illustrating a voltage level shifter according to another preferred embodiment of the present invention. Referring to FIG. 2, a NMOS transistor switch transistor 251 controlled by the control signal is provided for breaking the charging path. As a result, the voltage level of VOUT2B ~~VOUT1B~~ is maintained by the capacitor 221. FIG. 7 is a waveform diagram schematically illustrating the input and output voltages of the voltage level shifter of FIG. 2. Referring to FIG. 7, the voltage level of VOUT2B is maintained by the capacitor 221 when VA is changed to low voltage level.

Please amend paragraph [0041] as follows:

[0041]. Referring to FIG. 8, the PMOS transistor 301 ~~is turned~~ turns on when the clock TTL voltage signal remains at high level and, the control signals VA and VB provide a negative pulse and a positive pulse respectively. During this moment, the ~~PMOS~~ NMOS transistor 313 and the switch transistor 351 ~~are~~ turn off and VOUT3B remains at the same voltage level.

Please amend paragraph [0044] as follows:

[0044] As one preferred embodiment of the present invention, the two control signals VA and VB, for example, use positive and negative pulses as the controlling signals for a voltage level shifter. The control signals VA and VB are periodic signals. A negative pulse of VA and a positive pulse of VB are provided when the input TTL voltage signal VIN changes the state, wherein a width Twa of the negative pulse of VA corresponding to a delay after the rising of VIN. Thus, a narrower pulse width Twa is desired. Furthermore, a width Twb of the positive pulse of VB should be slightly wider than Twa because the time period Td will causes a high impedance state. The slightly wider negative pulse also can prevent from the conducting path constructed by the turning on of the PMOS transistors 303, 305 and the NMOS transistors 311, 313 and 351 when the input signal VIN is at high voltage level.

Please amend paragraph [0045] as follows:

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[0045] As another preferred embodiment of the present invention, the possible conducting paths, for example, can be constructed by the PMOS transistor 301, the NMOS transistor 313 and the switch transistor 351 during the changing of state thereof when VIN changes to high voltage level. Referring to FIG. ~~3~~ 9, the surge of current I(313) is much smaller than the surge of current I(415) because the PMOS transistor 301 and the NMOS transistor 313 are designed to be of any size.

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